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Amdt. sent July 7, 2004
Preliminary Amendment

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Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

1.   (Canceled)

1   2.   (New): A storage controller for exchanging user data between a host

2   system and a data storage unit comprising:

3   a microprocessor;

4   a local memory for a control program and for in-memory management

5   information; and

6   a cache memory for the user data, the cache memory storing therein in-cache

7   management information, the in-memory management information being representative of the

8   in-cache management information, the in-memory management information and the in-cache

9   management information each being information relating to user data that is stored in the cache

10   memory,

11   an access time between the microprocessor and the local memory to perform an

12   access operation being lower than an access time between the microprocessor and the cache

13   memory for the same access operation,

14   the control program configured to operate the microprocessor to process a read

15   request by performing steps of:

16   accessing the local memory to access the in-memory management

17   information;

18   based on the in-memory management information, determining whether

19   read-out data associated with the read request is stored in the cache memory;

20   if the read-out data is stored in the cache memory, then accessing the

21   cache memory to access the read-out data;

22   if the read-out data is not stored in the cache memory, then:

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23   accessing the data storage unit to access the read-out data;

24   storing the read-out data in the cache memory; and

25   updating the in-memory management information and the in-cache

26 management information to indicate an update of the cache memory.

1   3.   (New): The storage controller of claim 2 wherein the control program is

2 further configured to operate the microprocessor to process a write request by performing steps

3 of:

4   accessing the local memory to access the in-memory management information;

5   based on the in-memory management information, identifying a vacant area in the

6 cache memory;

7   storing write data associated with the write request into the vacant area; and

8   updating the in-memory management information and the in-cache management

9 information to indicate an update of the cache memory.

1   4.   (New): The storage controller of claim 2 wherein the local memory is

2 accessible only by the microprocessor.

1   5.   (New): The storage controller of claim 4 wherein the local memory is a

2 component of the microprocessor.

1   6.   (New): A subsystem comprising a storage control unit and a plurality of

2 storage units for storing data from a host computer, the storage control unit comprising:

3   a cache memory for user data that is transferred between the host computer and

4 the storage units; and

5   a processor operable to control the storage control unit, the processor having a

6 local memory for a control program and for management information relating to data stored in

7 the cache memory,

8   wherein the processor can access the local memory at a higher speed than the

9 cache memory,

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10   the control program configured to operate the processor to:

11   access the management information in the local memory, in response to a

12   write operation, to identify available space in the cache memory in order to store data

13   associated with the write operation; and

14   access the management information in the local memory, in response to a

15   read operation, to determine if requested data associated with the read operation is

16   contained in the cache memory, and if not then to:

17   access the management information in the local memory to

18   identify available space in the cache memory in order to store the requested data;

19   obtain the requested data from the storage units; and

20   store the requested data into the available space in the cache memory.

1   7.   (New): The subsystem according to claim 6 wherein the memory in the

2   processor is a volatile memory.

1   8.   (New): The subsystem according to claim 6 wherein the management

2   information is also stored in the cache memory.

1   9.   (New): The subsystem according to claim 8 wherein the processor

2   updates the management information in the cache memory together with the management

3   information in the processor.

1   10.   (New): The subsystem according to claim 6 wherein the storage units

2   have a RAID configuration.

1   11.   (New): The subsystem according to claim 6 wherein the storage units are

2   magnetic disk units.

1   12.   (New): A storage control unit for data communication with a plurality of

2   storage units and with at least one host computer comprising:

3   a first control unit for communication with the host computer;

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4   a second control unit for communication with the storage units;

5   a cache memory for user data being transferred between the host computer and

6   the storage units, the cache memory storing management information relating to user data that is

7   stored in the cache memory;

8   a data transfer control unit configured to transfer data between the first control

9   unit and the cache memory, and between the second control unit and the cache memory; and

10   a processor for controlling the storage control unit, the processor having therein a

11   local memory, for storing the management information,

12   wherein the processor, responsive to an operation to write data or to read data, is

13   configured:

14   to access the management information that is stored in the local memory;

15   to determine if the cache memory can accommodate the operation; and

16   if the cache memory can accommodate the operation, then to access the

17   cache memory to store the write data or the read data in the cache memory.

1   13.   (New): The storage controller according to claim 12 wherein the access

2   speed between the processor and the local memory is higher than the access speed between the

3   processor and the cache memory.

1   14.   (New): The storage controller according to claim 12 wherein the data

2   transfer control unit copies the management information from the cache memory to the local

3   memory.

1   15.   (New): The storage controller according to claim 12 wherein the data

2   transfer control unit copies the management information from the local memory to the cache

3   memory.

1   16.   (New): A subsystem comprising a storage control unit and a plurality of

2   storage units for storing data from a host computer wherein the storage control unit includes:

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3   a cache memory for temporarily storing data transferred between the host

4   computer and the storage units and for storing management information relating to user data that

5   is stored in the cache memory; and

6   a processor for controlling the storage control unit, the processor having therein a

7   local memory,

8   the processor being configured to store in the local memory at least a portion of

9   the management information relating to the data stored in the cache memory,

10   the processor further being configured to access the management information in

11   the local memory to determine if the cache memory can accommodate an operation to write data

12   or to read data and to access the cache memory to store write data or read data in the cache

13   memory if the cache memory can accommodate the operation.

1   17.   (New): The subsystem according to claim 16 wherein the memory in the

2   processor stores a control program for controlling the storage control unit.

1   18.   (New): The subsystem according to claim 16 wherein the local memory is

2   a volatile memory.

1   19.   (New): The subsystem according to claim 16 wherein the management

2   information includes at least one of a data attribute for managing the data in the cache memory, a

3   logical address of the data in the cache memory, available storage area information in the cache

4   memory, or management information regarding an order of priority of replacing contents of the

5   cache memory.

1   20.   (New): The subsystem according to claim 19 further comprising a data

2   transfer control unit for transferring the user data in the cache memory between the host

3   computer and the storage units.

1   21.   (New): The subsystem according to claim 16 wherein the processor

2   updates the management information in the cache memory and in the local memory.